REMARKS

Claims 1-10 and 25-44 are pending in the present application.

Due to the fact that the Examiner provided newly cited prior art that were not based upon previous amendments made to the claims, Applicant respectfully requests that the Examiner withdraw the finality of the present Final Office Action (dated January 19, 2006).

Applicant acknowledges and appreciates that the rejections based upon U.S. Patent No. 6,327,318 ***(Bhullar)***, U.S. Patent No. 6,323,705 ***(Shieh)***, and U.S. Patent No. 6,700,434 ***(Fujii)*** are withdrawn in view of the amendments and arguments presented in the Response to Office Action dated November 7, 2005.

The Examiner rejected claims 1-10 and 25-44 under 35 U.S.C. 112, second paragraph, as being indefinite. Applicant respectfully traverses this rejection.

Regarding claims 5, 29, and 37, the rejection under 35 U.S.C. 112, second paragraph is now moot in light of the amendments made to claims 5 and 29 (the first inverter, the transistor sets, and the second inverter are properly connected to elements in the claim). The Applicant believes that the Examiner mistakenly listed claim 37 in this category since claim 37 does not recite a first inverter, second inverter, or a transistor set. Therefore, claims 5, 29, and 37 are allowable.

Regarding claims 1, 25, and 35, Applicant respectfully traverses the Examiner's rejection under 35 U.S.C. 112, second paragraph. The Examiner objected to the use of the term "switch". However, Applicant respectfully asserts that this term would be readily understood by those skilled in the art having benefit of the present disclosure. Additionally, in order to move

prosecution forward, Applicant has amended the claims 1, 25, and 35 to address the Examiner's concerns. Therefore, claims 1, 25, and 35 are now allowable.

In light of the Amendments and arguments provided herein, Applicant respectfully asserts that the rejections under 35 U.S.C. 112, second paragraph, are now moot, and that claims 1-10 and 25-44 are allowable.

The Examiner rejected claims 1-4, 9-10, 35-36 and 43-44 under 35 USC 102(b) as being anticipated by U.S. Patent 6,483,359 ***(Lee)***. Applicant respectfully traverses this rejection.

Applicants respectfully assert that all of the elements of independent claims 1 and 35 (both as amended) are not taught, disclosed, or suggested by ***Lee***. The Examiner merely listed a few elements, such as a phase detector, a first delay line and a second delay line and a feedback line of ***Lee*** to assert anticipation of claims 1 and 35. The Examiner merely provides conclusary statements equating the delay lines of ***Lee*** to the course delay circuit and the fine delay called for by claims of the present invention. In other words, the Examiner merely lists various reference numbers next to certain words out of the elements of claims of the present invention. Applicants respectfully assert that ***Lee*** does not teach, disclose or suggest all of the elements of claims 1 and 35 (as amended) of the present invention.

Presumably, the Examiner is viewing the capacitors C1, C2, C3, in Figures 4, and 6A thru 6D of ***Lee*** to argue anticipation of elements of the claims of the present invention. However, Applicant respectfully asserts that claim 1 and 35 of the present invention call for a delay lock loop that comprises a delay circuit for activating a <u>transitive</u> capacitive delay. In contrast, the disclosure of ***Lee*** merely refers to a passive capacitor that may be connected to the inverted clock signal, as described in Figures 4 and 6A-6D of ***Lee***. The Examiner provides no

explanation or arguments as to how the disclosure of ***Lee*** anticipates elements of claims of the present invention. Further, ***Lee*** simply does not disclose a transitive capacitive delay, as called for by claims 1 and 35 of the present invention. Various advantages of implementing the present invention is achieved over the prior art. For example, the Specification discloses the issue of an RC time constant that may become problematic when applying the standard passive capacitor, as disclosed by ***Lee***. Further, utilizing the transitive capacitive elements, an advantage of providing for a relatively constant capacitance during voltage transitions may be achieved, which is a feature that is not provided by ***Lee***. *See* Specification, p.19, lines 3-15. Therefore, various exemplary advantages may be achieved utilizing the transitive capacitive disclosed by claims 1 and 35. ***Lee*** simply does not disclose activating a transistive capacitive delay, as called for claims 1 and 35 of the present invention. Therefore, ***Lee*** clearly does not anticipate all of the elements of claims 1 and 35 of the present invention. Accordingly, independent claims 1 and 35 of the present invention are allowable for at least the reasons cited herein. Further claims 2-10 and 36-44, which depend from independent claims 1 and 35, respectively, are also allowable for at least the reasons cited herein.

The Examiner rejected claims 25-28 and 33-34 under 35 USC 103(a) as being unpatentable over U.S. Patent 5,831,929 ***(Manning)*** in view of ***Lee.*** Applicant respectfully traverses this rejection.

Applicant respectfully asserts that independent claim 25 is not taught, disclosed, or made obvious by ***Manning***, ***Lee***, or their combination. The Examiner cites ***Manning*** to make obvious the element of a first device and a second device of claim 25. Firstly, ***Manning*** does even disclose what the Examiner purports. Secondly, ***Manning*** has deficiencies that are not made up for by ***Lee***, as described below.

Contrary to Examiner's assertions, ***Manning*** does not disclose a system board that comprises a first device and a second device, as recited in claim 25 of the present invention. In fact, ***Manning*** does not disclose a first and a second device at all. ***Manning*** merely discloses a single memory device that includes various *portions or sections*, such as a memory array and a memory controller. The Examiner merely asserts that the memory array 46 in the memory system or device 38 makes obvious the second device and the memory controller 44 makes obvious the first device. These elements are merely components of a *packetized* memory system 38. In other words, they are just components of a memory device. The memory array 46 and the memory controller 44 allegedly purported make obvious the first and second device are merely components of a single, packetized memory product. *See* Figure 1 and column 1, lines 33-36. Therefore, ***Manning*** simply does not disclose a first device comprising a memory location for storing data and a data lock loop and a second device to access said data. The memory controller 44 of ***Manning*** is merely directing data from the array 46 to be accessed by a different device that may access memory from the packetized memory product 38. Therefore, ***Manning*** simply does not disclose or make obvious the first device and the second device called for by claim 25 of the present invention.

Additionally, *arguendo*, even if ***Manning*** disclosed the first and second devices, ***Manning*** simply does not disclose or make obvious providing the DLL circuit for performing the delay switching, much less the capacitive delay activation called for by claim 25. In fact, ***Manning***, as the Examiner admitted, does not disclose the DLL circuit comprising delay, as recited by claim 25. Simply adding the disclosure of ***Lee*** would still not make up for the deficit of ***Manning*** since ***Manning*** does not disclose the first and the second device, as described above.

Further, without hindsight reasoning, those skilled in the art simply would not combine ***Manning*** and ***Lee*** to make obvious all of the elements of claim 25 of the present invention. ***Lee*** is directed to a delay lock loop for use in a semiconductor memory device. In contrast, ***Manning*** is directed to a memory device with staggered data paths. ***Manning*** is simply directed to data transferring to data paths or to a memory array of a memory product, wherein ***Lee*** is directed to a delay lock loop. Simply because both cited art deal with memory, would not cause those skilled in the art to find motivation to combine them to make obvious all of the elements of claim 25 of the present invention. The Examiner provides no argument to support this rejection, nor is there any evidence to indicate that those skilled in the art would combine ***Lee*** and ***Manning*** comb to make obvious all of the elements of claim 25 of the present invention. There is no evidence or arguments to the contrary. Further, as described above, even if ***Manning*** and ***Lee*** were to be combined, all of the elements would still not be taught, disclosed or made obvious of claim 25. Therefore, claim 25 of the present invention is allowable.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, the prior art reference (or references when combined) must teach or suggest all the claim limitations. As described above, the combination of ***Lee*** and ***Manning*** do not teach or suggest all of the elements of claim 25 of the present invention.

Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Applicant respectfully asserts that the Examiner has provided no evidence nor any evidence in the cited prior art that would provide an indication of motivation of those skilled in the art to combine ***Lee*** and ***Manning*** to read upon all of the elements of claim 25 of the present invention. Without improper hindsight, those skilled in the art simply would

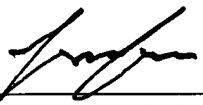
not find the motivation to combine the delay lock loop of ***Lee*** with the data path disclosure of ***Manning*** to make obvious all of the elements of claim 25 Therefore, there is no evidence or motivation, either in the references themselves or in the knowledge, generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings.

Third, there must be a reasonable expectation of success. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on appellant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991); M.P.E.P. § 2142. There is no evidence that the improbable combination of ***Lee*** and ***Manning*** provide a reasonable expectation of success. There is no evidence to a contrary assertion, and the Examiner fails to provide any evidence of reasonable expectation of success based upon the prior art. Therefore, the Examiner failed to establish a *prima facie* evidence of obviousness with respect to claim 25 of the present invention. Accordingly, for a least the reasons described above ***Lee*** and ***Manning*** do not cause all of the elements of claim 25 to be are taught, disclosed, or suggested. Accordingly, independent claim 25 is allowable. Further, dependent claims 26-34, which depend from claim 25, are also allowable for at least the reasons cited herein.

Applicant acknowledges and appreciates that the Examiner indicated that claims 5-8, 29-32 and 37-42 contain allowable subject matter. However, in light of the arguments and amendments provided herein, Applicant respectfully asserts that all pending claims of the present application are allowable. Therefore, Applicant respectfully solicits a Notice of Allowance, allowing claims 1-10 and 25-44 of the present invention.

Reconsideration of the present application is respectfully requested.

If for any reason the Examiner finds the application other than in condition for allowance, the **Examiner is requested to call the undersigned attorney** at the Houston, Texas, telephone number (713) 934-4069 to discuss the steps necessary for placing the application in condition for allowance.

Date: March 20, 2006	Respectfully submitted, WILLIAMS, MORGAN & AMERSON, P.C. CUSTOMER NO. 23720 By:  Jaison C. John, Reg. 50,737 10333 Richmond, Suite 1100 Houston, Texas 77042 (713) 934-4069 (713) 934-7011 (facsimile) ATTORNEY FOR APPLICANT(S)